

FIG. 2

0073458-424800

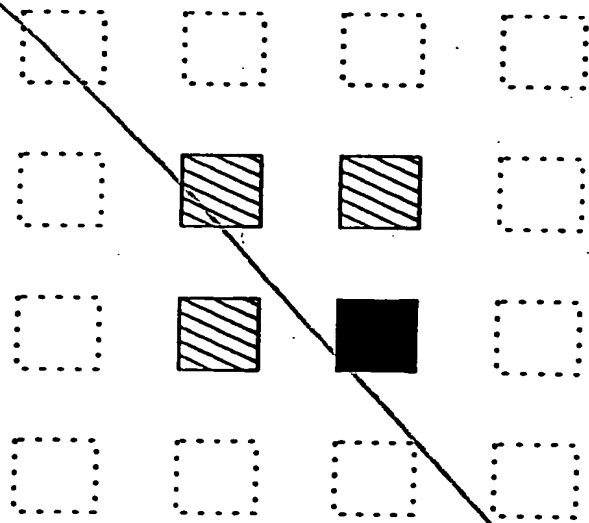


FIG. 3

Input data
block

A priori or side information

Reversible Preprocessor

410

25

Standard source input

~~Adaptive variable
length coder~~

420

**Coded
Block**

400

FIG. 4

003727 8976260

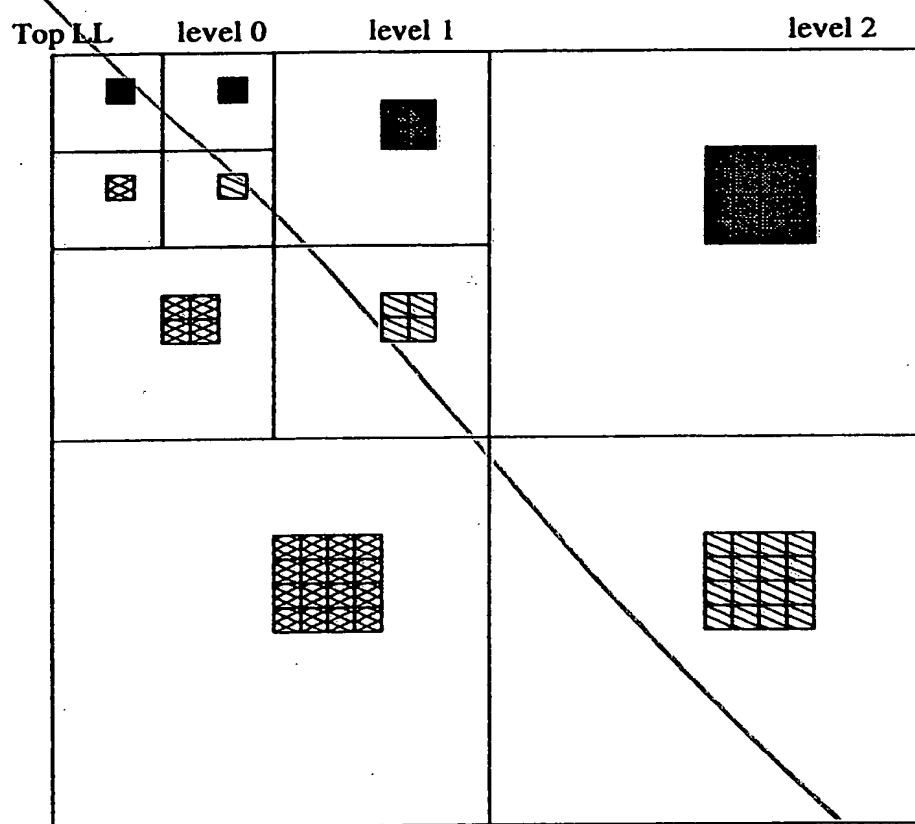


FIG. 5

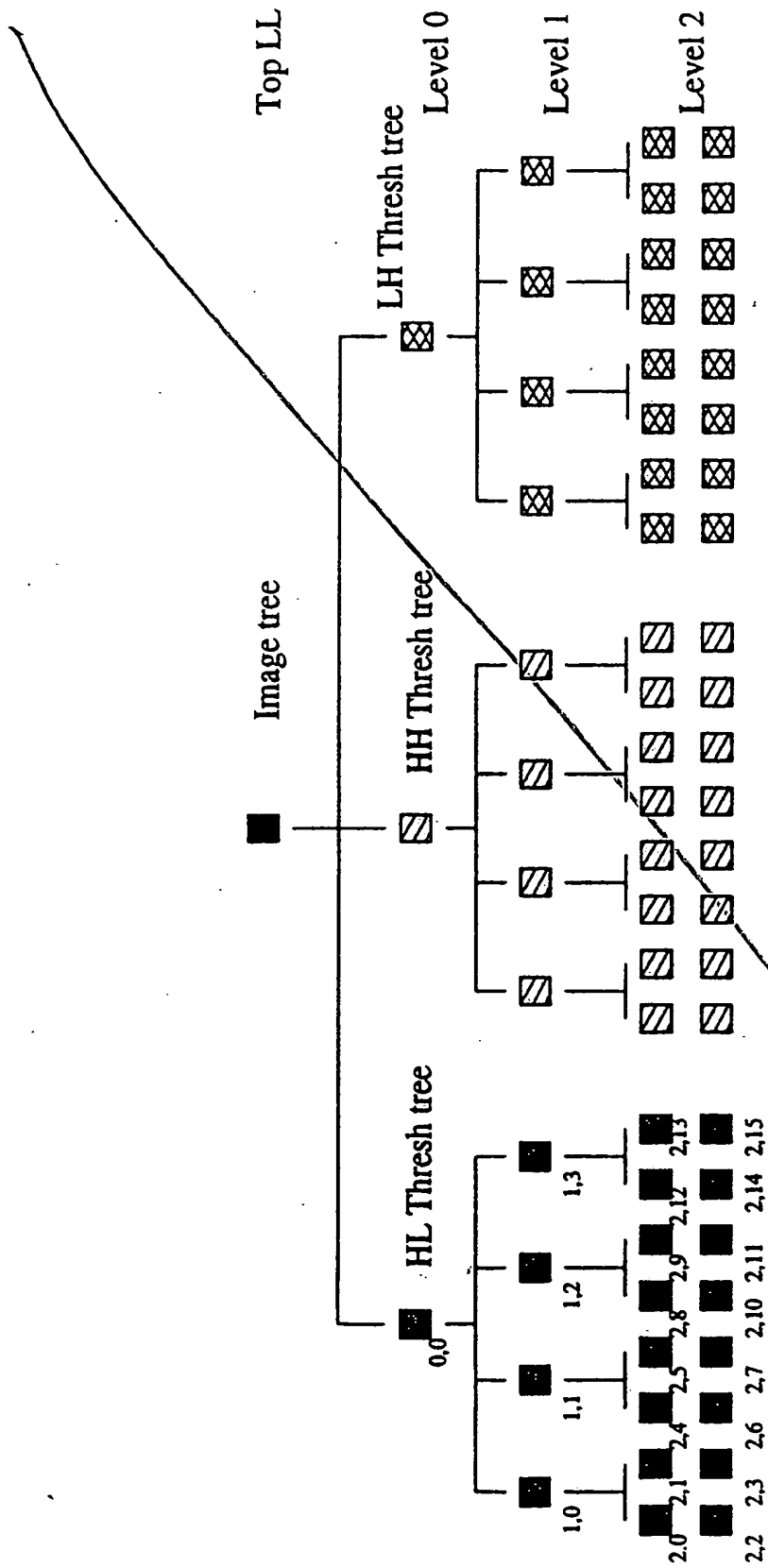


FIG. 6

700

702'

704'

706'

708'

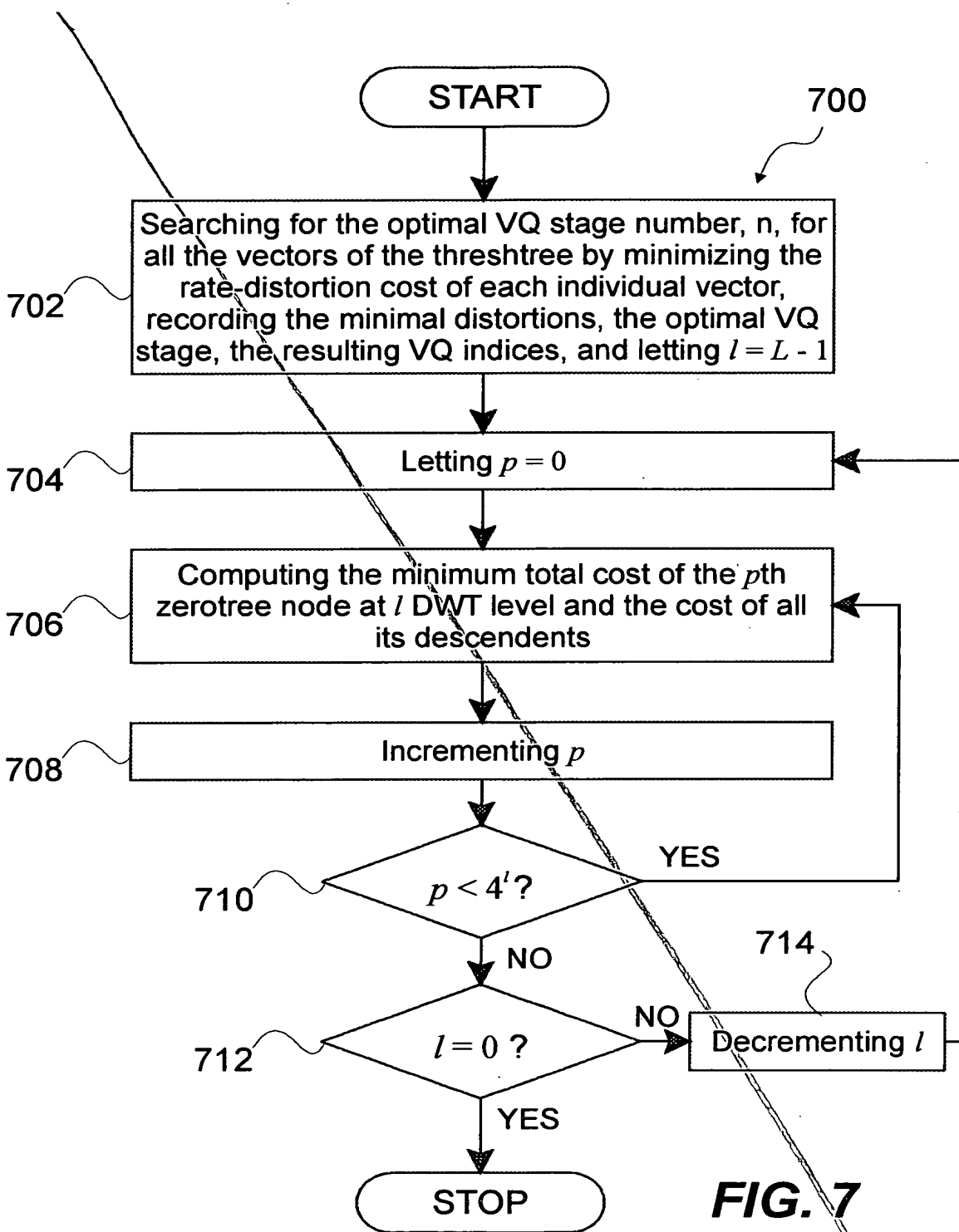
710

714

712

NO

FIG. 7



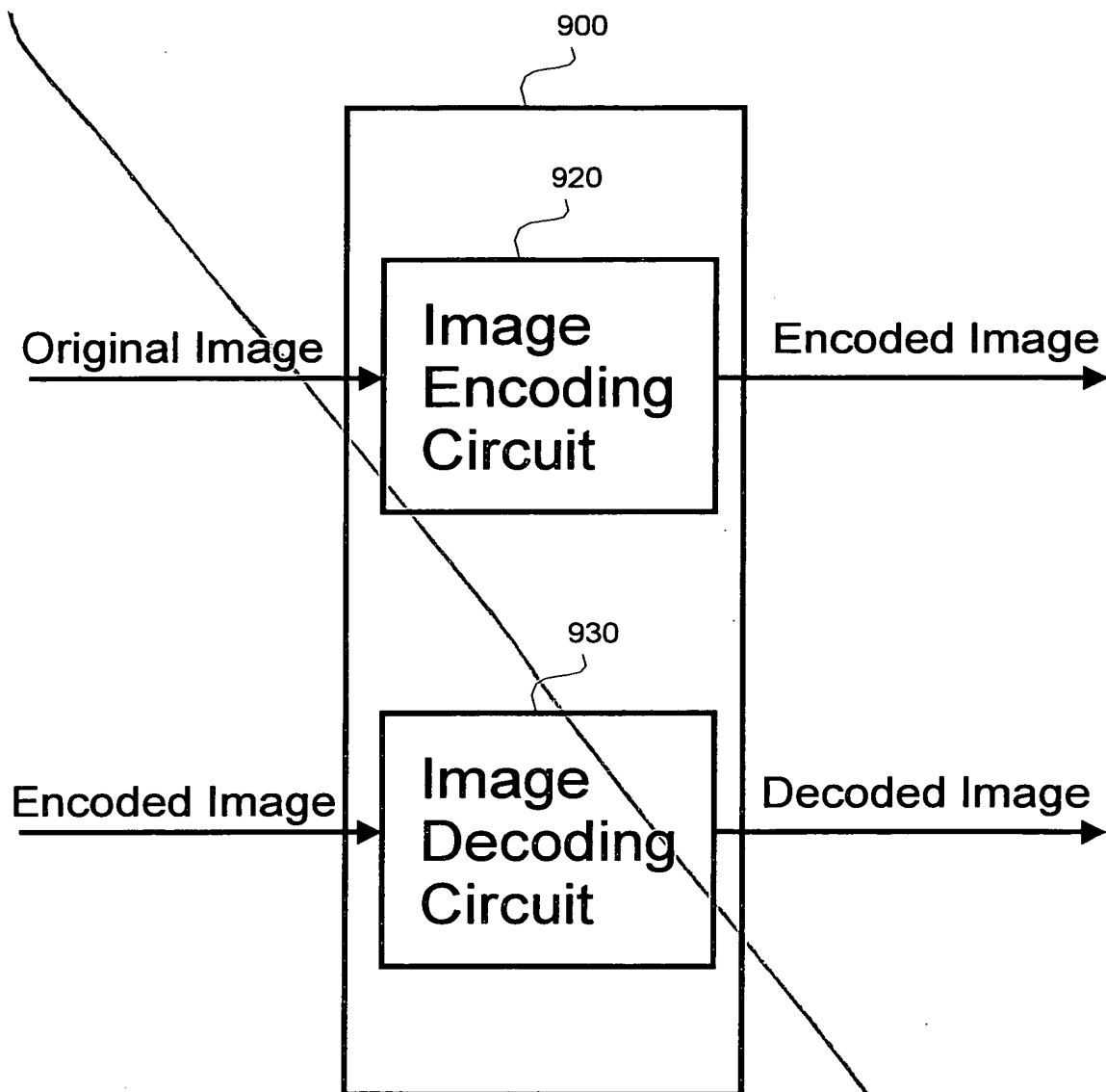


FIG. 9


```

graph LR
    52[Input Device] --> 54[Processor Device]
    54 --> 56[Output Device]
    54 <--> 58[Storage Device]
    54 <--> 60[Memory Device]

```

FIG. 11